

## Claims

- 1        1. A wafer, comprising:
  - 2                an array of chips having contacts, said contacts comprising solder bumps, said
  - 3                array of chips including perimeter chips extending along a periphery of the wafer;
  - 4                and
  - 5                additional dummy solder bumps located adjacent most of said perimeter chips
  - 6                wherein said additional dummy solder bumps are for improving contact
  - 7                processing of said perimeter chips.
- 1        2. The wafer as recited in claim 1, wherein said additional dummy solder bumps are for
- 2                providing support for a shadow mask used to deposit a material on said solder bumps
- 3                so said shadow mask does not damage perimeter chip solder bumps.
- 1        3. The wafer as recited in claim 2, wherein said solder bumps comprise a layer of said
- 2                material.
- 1        4. The wafer as recited in claim 3, wherein said material comprises tin.
- 1        5. The wafer as recited in claim 3, wherein said material is deposited on reflowed
- 2                bumps.
- 1        6. The wafer as recited in claim 1, wherein said additional dummy solder bumps are
- 2                omitted in saw blade lanes.
- 1        7. The wafer as recited in claim 6, wherein said additional dummy solder bumps are
- 2                omitted in a ring shaped exclusion region along said periphery of the wafer.

- 1        8. The wafer as recited in claim 7, wherein said additional dummy solder bumps are  
2        omitted in regions of alignment aids.
- 1        9. The wafer as recited in claim 8, wherein said alignment aids comprise a pattern of  
2        solder bumps.
- 1        10. The wafer as recited in claim 9, wherein said pattern of solder bumps comprises a  
2        pattern having a closer spacing of solder bumps than is used for contacts.
- 1        11. The wafer as recited in claim 7, wherein said additional dummy solder bumps  
2        adjacent a perimeter chip are arranged in a regular array of bumps with all positions of  
3        said array outside said saw blade lanes and said exclusion zone filled.
- 1        12. The wafer as recited in claim 1, wherein said additional dummy solder bumps  
2        comprise a single row of bumps adjacent said perimeter chips.
- 1        13. The wafer as recited in claim 1, wherein said additional dummy solder bumps  
2        comprise additional patterns of bumps corresponding to partial chips.
- 1        14. The wafer as recited in claim 1, wherein said improving contact processing of said  
2        perimeter chips is more uniform plasma etching of insulator in contacts on the wafer  
3        and lower contact resistance for perimeter chips.
- 1        15. The wafer as recited in claim 1, wherein contacts of said perimeter chips have contact  
2        resistance about equal to that of non-perimeter chips.
- 1        16. The wafer as recited in claim 1, wherein contacts of said perimeter chips have  
2        insulator about equal to that of non-perimeter chips.

3 17. A shadow mask, comprising:

4 an array of holes in the shadow mask corresponding to contacts on an array of  
5 chips on a wafer, said array of chips including perimeter chips extending along a  
6 periphery of the wafer; and

7 additional dummy holes in the shadow mask located adjacent holes corresponding  
8 to most of said perimeter chips wherein said additional dummy holes are for  
9 improving contact processing of said perimeter chips.

✓  
1 18. The shadow mask as recited in claim 17, wherein said additional dummy holes are for  
2 providing additional dummy solder bumps to support a second shadow mask used to  
3 deposit an additional layer of material on said solder bumps so said second shadow  
4 mask does not damage perimeter chip solder bumps.

1 19. The shadow mask as recited in claim 18, wherein said holes for depositing said  
2 additional layer of material are located in positions to compensate for the temperature  
3 of depositing tin.

1 20. The shadow mask as recited in claim 18, wherein said additional layer of material is  
2 for depositing through said second shadow mask onto reflowed solder bumps on  
3 chips.

1 21. The shadow mask as recited in claim 17, wherein said additional dummy holes are  
2 omitted in saw blade lanes. *per*

1 22. The shadow mask as recited in claim 21, wherein said additional dummy holes are  
2 omitted in a ring shaped exclusion zone along said periphery of the shadow mask  
3 beyond said perimeter chips and beyond said dummy holes. *noted*

1 ✕ 23. The shadow mask as recited in claim 17, wherein said improved contact processing of  
2 said perimeter chips is improved removal of insulator in contacts of said perimeter  
3 chips and lower contact resistance for said perimeter chips.

1 24. The shadow mask as recited in claim 17, wherein said additional dummy holes are  
2 located adjacent holes for substantially all of said perimeter chips.

1 25. The shadow mask as recited in claim 17, wherein said holes corresponding to said  
2 perimeter chips are located to compensate for the temperature of depositing chrome,  
3 copper, or gold.

1        26. A method of fabricating a semiconductor wafer, comprising the steps of:

2            (a) providing a wafer comprising an array of chips having contacts, said contacts  
3                comprising solder bumps, said array of chips including perimeter chips extending  
4                along a periphery of the wafer; and

5            (b) providing additional dummy solder bumps located adjacent most of said perimeter  
6                chips wherein said additional dummy solder bumps are for improving contact  
7                processing of said perimeter chips.

1        27. A method of fabricating a semiconductor wafer as recited in claim 26, wherein said  
2            step (b) comprises the steps of:

3            1. providing a wafer comprising contacts;

4            2. providing a shadow mask comprising additional holes corresponding to said  
5                additional dummy solder bumps, and aligning holes of said mask with  
6                contacts of said wafer;

7            3. plasma etching oxide in said contacts through said holes in said mask, wherein  
8                oxide in contacts of perimeter chips is etched about as well as contacts of non-  
9                perimeter chips as a result of the presence of said additional holes; and

10          4. depositing ball limited metallurgy and solder for solder bumps in said holes.

1        28. The method of fabricating a semiconductor wafer as recited in claim 27, wherein  
2            said improved contact processing of said perimeter chips is more uniform plasma  
3            etching of oxide in contacts on the wafer and lower contact resistance for perimeter  
4            chips.

1 29. The method of fabricating a semiconductor wafer as recited in claim 28, wherein  
2 contacts of said perimeter chips have contact resistance about equal to that of non-  
3 perimeter chips.

1 30. The method of fabricating a semiconductor wafer as recited in claim 28, wherein  
2 contacts of said perimeter chips have oxide about equal to that of non-perimeter  
3 chips.

1 31. The method of fabricating a semiconductor wafer as recited in claim 27, further  
2 comprising the step of reflowing said solder bumps.

1 32. The method of fabricating a semiconductor wafer as recited in claim 31, further  
2 comprising providing a solder bump cap shadow mask, wherein said step (b) of  
3 providing additional dummy solder bumps is for providing support for said solder  
4 bump cap shadow mask used to deposit a material on said solder bumps so said  
5 solder bump cap shadow mask does not damage perimeter chip solder bumps.

1 33. The method of fabricating a semiconductor wafer as recited in claim 32, further  
2 comprising depositing a layer of said material on said solder bumps through said  
3 solder bump cap shadow mask.

1 34. The method of fabricating a semiconductor wafer as recited in claim 33, wherein  
2 said material comprises tin.

1 35. The method of fabricating a semiconductor wafer as recited in claim 26, wherein  
2 said additional dummy solder bumps are omitted in saw blade lanes.

1        36. The method of fabricating a semiconductor wafer as recited in claim 26, wherein  
2            said additional dummy solder bumps are omitted in a ring shaped exclusion zone  
3            along said periphery of the wafer.

1        37. The method of fabricating a semiconductor wafer as recited in claim 26, wherein  
2            said additional dummy holes are located adjacent holes for substantially all of said  
3            perimeter chips.

1        38. A method of fabricating a shadow mask, comprising the steps of:

2            a) providing an array of holes in the shadow mask corresponding to contacts on

3            an array of chips on a wafer, said array of chips including perimeter chips

4            extending along a periphery of the wafer; and

5            b) providing additional dummy holes in the shadow mask located adjacent holes

6            corresponding to most of said perimeter chips wherein said additional dummy

7            holes are for improving contact processing of said perimeter chips.

1        39. The method of fabricating a shadow mask as recited in claim 38, wherein said

2            improved contact processing of said perimeter chips is additional dummy solder

3            bumps to support a second shadow mask used to deposit an additional layer of

4            material on said solder bumps so said second shadow mask does not damage

5            perimeter chip solder bumps.

1        40. The method of fabricating a shadow mask as recited in claim 38, wherein said

2            additional dummy holes are omitted in saw blade lanes.

1        41. The method of fabricating a shadow mask as recited in claim 40, wherein said

2            additional dummy holes are omitted in a ring shaped exclusion zone along said

3            periphery of the shadow mask beyond said perimeter chips and beyond said dummy

4            holes.

1        42. The method of fabricating a shadow mask as recited in claim 40, further comprising

2            the step of inspecting the mask using dummy holes along an edge of a dicing lane to

3            align the shadow mask to an inspection device.



1       43. The method of fabricating a shadow mask as recited in claim 40, further comprising  
2       the step of inspecting the mask using a pattern of additional holes, said additional  
3       holes located beyond holes corresponding to said perimeter chips, said additional  
4       holes for aligning the shadow mask to an inspection device, wherein said pattern of  
5       additional holes does not print on the wafer.

1       44. The method of fabricating a shadow mask as recited in claim 43, wherein said  
2       pattern of additional holes is located so that it will be covered by a guard ring.

1       45. The method of fabricating a shadow mask as recited in claim 40, further comprising  
2       the step of inspecting the mask using a covering for said additional dummy holes.

1       46. The method of fabricating a shadow mask as recited in claim 40, wherein said  
2       covering for said additional dummy holes is a ring having an inside edge  
3       corresponding to outside edges of perimeter chips.

1       47. The method of fabricating a shadow mask as recited in claim 38, wherein said  
2       improved contact processing of said perimeter chips is more uniform plasma etching  
3       of contacts on the wafer and lower contact resistance for perimeter chips.

- 1        48. A wafer, comprising:
- 2                an array of chips having solder bump contacts; and
- 3                a pattern of solder bumps for aligning the wafer with a solder bump deposition
- 4                mask, the pattern of solder bumps comprising bumps having dimensions about
- 5                equal to or smaller than said solder bump contacts.
- 1        49. The wafer as recited in claim 48, wherein said aligning solder bumps has a closer
- 2                spacing than do said solder bump contacts.
- 1        50. The wafer as recited in claim 48, wherein said aligning solder bumps are located so
- 2                as to correspond to edges of a second alignment pattern on the wafer.